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PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10030435	01/10/2002	156	306.6	1733 ~~1734~~	Goff

**APPLICANTS: Kariya Takashi;

**CONTINUING DATA VERIFIED:
THIS APPLICATION IS A 371 OF PCT/JP00/08105 11/16/2000

** FOREIGN APPLICATIONS VERIFIED:
JAPAN 2000-137144 05/10/2000

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no		217883US3PCT
Verified and Acknowledged Examiners's intials			

TITLE : Method of producing multilayer circuit boards

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE			DRAWING	
Amount Due	Date Paid		Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAMER		Primary Examiner	Application Examiner	
		PREPARED FOR ISSUE		

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